Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (original): A multi-service segmentation and reassembly (MS-SAR) integrated circuit, comprising:

a first bus interface;

lookup circuitry;

segmentation circuitry;

reassembly circuitry;

a second bus interface; and

a data path extending from the first bus interface to the lookup circuitry, and from the lookup circuitry to the segmentation circuitry, and from the segmentation circuitry to the reassembly circuitry, and from the reasssembly circuitry to the second bus interface, wherein both cell-protocol traffic and packet-protocol traffic pass over the data path from the first bus interface, through the lookup circuitry, through the segmentation circuitry, through the reassembly circuitry and out of the integrated circuit from the second bus interface, the lookup circuitry analyzing the cell-protocol traffic and outputting information that causes the cell-protocol traffic to be processed in a first way by the segmentation circuitry and the reassembly circuitry, the lookup circuitry analyzing the packet-protocol traffic and outputting information that causes the packet-protocol traffic to be processed in a second way by the segmentation circuitry and the reassembly circuitry.

Claim 2 (original): The integrated circuit of claim 1, wherein the integrated circuit is operable in a first ingress mode such that traffic is output from the integrated circuit to a cell-based switch

fabric via the second bus interface, and wherein the integrated circuit is operable in a second ingress mode such that traffic is output from the integrated circuit to a packet-based switch fabric via the second bus interface.

Claim 3 (original): The integrated circuit of claim 1, wherein the integrated circuit is operable in a first egress mode such that traffic is received onto the integrated circuit from a cell-based switch fabric via the first bus interface, and wherein the integrated circuit is operable in a second egress mode such that traffic is received onto the integrated circuit from a packet-based switch fabric via the first bus interface.

Claim 4 (original): The integrated circuit of claim 1, wherein the integrated circuit is operable in an ingress mode such that traffic is output from the integrated circuit to a switch fabric via the second bus interface, and wherein the integrated circuit is operable in an egress mode such that traffic is received onto the integrated circuit from a switch fabric via the first bus interface.

Claim 5 (original): The integrated circuit of claim 1, wherein: 1) the integrated circuit is operable in a first ingress mode such that traffic is output from the integrated circuit to a cell-based switch fabric via the second bus interface, 2) the integrated circuit is operable in a second ingress mode such that traffic is output from the integrated circuit to a packet-based switch fabric via the second bus interface, 3) the integrated circuit is operable in a first egress mode such that traffic is received onto the integrated circuit from a cell-based switch fabric via the first bus interface, and 4) the integrated circuit is operable in a second egress mode such that traffic is received onto the integrated circuit from a packet-based switch fabric via the first bus interface.

Claim 6 (original): The integrated circuit of claim 1, wherein the cell-protocol traffic is ATM traffic, and wherein the packet-protocol traffic is MPLS traffic.

Claim 7 (original): The integrated circuit of claim 1, further comprising:

memory manager circuitry, wherein the data path extends from the segmentation circuitry to the reassembly circuitry via the memory manager circuitry.

Claim 8 (original): The integrated circuit of claim 1, wherein the cell-protocol traffic involves an ATM cell, and wherein the packet-protocol traffic involves a packet, the ATM cell being temporarily stored in one of a plurality of buffers of a memory, all of the buffers being of equal size, the packet being segmented into a plurality of chunks, and each of the chunks being temporarily stored into a corresponding one of the buffers.

Claim 9 (currently amended): An integrated circuit comprising:

a first bus interface;

means for generating a segmentation trailer;

means for checking a segmentation trailer;

a second bus interface; and

a data path extending from the first bus interface to the means for generating, and from the means for generating to the means for checking, and from the means for checking to the second bus interface, wherein both cell-protocol traffic and packet-protocol traffic pass over the data path from the first bus interface, through means for generating, through the means for checking, and out of the integrated circuit from the second bus interface.

Claim 10 (currently amended): The integrated circuit of claim 9, wherein the integrated circuit is operable in an ingress mode and in an egress mode,

wherein in the ingress mode the integrated circuit is adapted for segmenting a packet into a plurality of segments, the means for generating a segmentation trailer generating a segmentation trailer and appending the segmentation trailer to one of the segments, the segments being output from the integrated circuit in the form of switch cells, and

wherein in the egress mode the integrated circuit is adapted for outputting packet information such that the packet information is transmitted as a packet onto a network, the means for checking receiving a plurality of segments, a last one of the plurality of segments including a segmentation trailer, the means for ~~checking~~ checking the segmentation trailer.

Claim 11 (original): A switching device, comprising:

a first multi-service segmentation and reassembly (MS-SAR) integrated circuit;

a switch fabric; and

a second multi-service segmentation and reassembly (MS-SAR) integrated circuit, a flow of network information passing into the first MS-SAR, and then through the first MS-SAR, and then through the switch fabric, and then through the second MS-SAR, and then out of the second MS-SAR, wherein the flow passing into the first MS-SAR is of a first traffic type, and wherein the flow passing out of the second MS-SAR is of a second traffic type, wherein the switching device can process the flow for all the four following pairs of first and second traffic types: 1) the first traffic type is ATM and the second traffic type is ATM, 2) the first traffic type is ATM and the second traffic type is packet, 3) the first traffic type is packet and the second traffic type is ATM, and 4) the first traffic type is packet and the second traffic type is packet, wherein the first and second MS-SAR integrated circuits are substantially identical integrated circuits.

Claim 12 (original): The switching device of claim 11, wherein when the first traffic type is ATM and the second traffic type is packet then the ATM traffic type involves AAL5 adaptation layer cells, and wherein when the first traffic type is packet and the second traffic type is ATM then the ATM traffic type involves AAL5 adaptation layer cells.

Claim 13 (original): The switching device of claim 11, wherein the switching device can also process a flow such that a single ATM cell is received onto the first MS-SAR and that ATM cell is output from the second MS-SAR encapsulated in a packet, there only being one ATM cell encapsulated in the packet.

Claim 14 (original): The switching device of claim 11, wherein the switching device can also process a flow such that a packet that encapsulates a single ATM cell is received onto the first MS-SAR, and wherein the ATM cell is de-encapsulated and output from the second MS-SAR as an ATM cell.

Claim 15 (original): The switching device of claim 11, wherein the switching device in an OSI layer three Internet Protocol (IP) router.

Claim 16 (original): The switching device of claim 11, wherein the switching device is an OSI layer two switch that does not perform Internet Protocol (IP) routing.

Claim 17 (currently amended): A multi-service segmentation and reassembly (MS-SAR) integrated circuit capable of processing, in a data path, a flow received from a switch fabric in accordance with a first egress application type or in accordance with a second egress application type, an indication of an application type being present in the flow as the flow is received onto the MS-SAR, the MS-SAR locating the indication and if the indication indicates the first egress application type then the MS-SAR processes the flow in the data path in accordance with the first egress application type, but if the indication indicates the second egress application type then the MS-SAR processes the flow in the data path in accordance with the second egress application type.

Claim 18 (original): The MS-SAR of claim 17, wherein the flow is received on the MS-SAR in the form of a switch cell, the switch cell including a switch header, the indication of an application type being a plurality of bits in the switch header.

Claim 19 (original): The MS-SAR of claim 17, wherein the flow is received from one of a plurality of input ports, each of the plurality of input ports having a port identification number (port ID), the MS-SAR having, for each of the plurality of input ports, access to locating information on where in a flow received on that input port the indication of application type would be located, the MS-SAR using the port ID of a flow to access the locating information, the MS-SAR using the locating information to locate in the flow the indication of application type.

Claims 20-33 (cancelled)